

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 54. Please amend claims 46, 49, 51, 52, 60, and 65, as follows:

Listing of Claims:

1-43. (Cancelled)

44. (Previously presented) A semiconductor structure, comprising:  
a substrate having a trench formed therein and further having a surface;  
an isolation pad formed in the trench and having an upper surface extending from the surface of the substrate;

a gate structure formed on the surface of the substrate and laterally displaced from the isolation pad, the gate structure having a gate oxide, a first gate layer, and a second gate layer formed on the first gate layer, the second gate layer of the gate structure having an upper surface at a first height relative to the surface of the substrate;

a component structure at least partially formed on the isolation pad, the part of the component structure formed on the isolation pad formed from the second gate layer that has an upper surface at a second height relative to the surface of the substrate surface less than the first height.

45. (Previously presented) The semiconductor structure of claim 44 wherein the second gate layer of the component structure is formed on the upper surface of the isolation pad.

46. (Currently amended) The semiconductor structure of claim 44, further comprising an oxide spacer formed adjacent the gate structure wherein the second gate layer of the gate structure has a first thickness and the second gate layer of the component structure has a second thickness greater than the first thickness.

47. (Previously presented) The semiconductor structure of claim 44 wherein the first gate layer has a first gate layer height relative to the surface of the substrate greater than a height of the upper surface of the isolation pad relative to the surface of the substrate.

48. (Previously presented) The semiconductor structure of claim 44 wherein the first gate layer has a first gate layer height relative to the surface of the substrate less than the second height.

49. (Currently amended) A semiconductor structure, comprising:  
a substrate having a trench formed therein and further having a surface;  
an isolation pad formed in the trench and having an upper surface extending from the surface of the substrate;

a gate structure formed on the surface of the substrate and laterally displaced from the isolation pad, the first-gate structure having a gate oxide, a first gate layer, and a second gate layer formed on the first gate layer, the first second-gate layer of the gate structure having a first gate layer height relative to the surface of the substrate thickness;

a component structure at least partially formed on the isolation pad, the part of the component structure formed on the isolation pad ~~formed~~ from the second gate layer having a ~~that has a~~ second gate layer height relative to the surface of the substrate thickness greater than the first thickness-gate layer height.

50. (Previously presented) The semiconductor structure of claim 49 wherein the second gate layer of the component structure is formed on the upper surface of the isolation pad.

51. (Currently amended) The semiconductor structure of claim 49 wherein the ~~first gate layer has a~~ first gate layer height is relative to the surface of the substrate greater than a height of the upper surface of the isolation pad relative to the surface of the substrate.

52. (Currently amended) The semiconductor structure of claim 49 wherein the second gate layer over the first gate layer has a first gate layer height relative to the surface of the substrate and the second gate layer of the component structure formed on the isolation pad has a second height relative to the surface of the substrate greater than the second first gate layer height.

53-56. (Cancelled)

57. (Previously presented) The microelectronic device of claim 59, further comprising a silicide layer formed over the polysilicon adhesion layer.

58. (Previously presented) The microelectronic device of claim 59, further comprising a tungsten silicide layer formed over the polysilicon adhesion layer.

59. (Previously presented) A microelectronic device, comprising:  
a microelectronic substrate;  
a gate oxide layer formed on the substrate;  
a polysilicon gate layer formed on the gate oxide layer;  
a trench defined through the polysilicon gate layer, the gate oxide layer and extending into the substrate;

a field oxide in the trench, the field oxide having a field oxide level between a level of an upper surface of the gate oxide and a level of an upper surface of the polysilicon gate layer; and

a polysilicon adhesion layer formed over the polysilicon gate layer and the upper surface of the field oxide, the polysilicon adhesion layer has an upper surface over the upper surface of the field oxide below the upper surface of the polysilicon adhesion layer over the polysilicon gate layer.

60. (Currently amended) The microelectronic device of claim 59 wherein the upper surface of the polysilicon adhesion layer is below ~~has a first thickness over~~ the upper surface of the ~~field oxide and having a second thickness less than the first thickness over the~~ polysilicon gate layer polysilicon adhesion layer over the upper surface of the field oxide.

61. (Previously presented) A microelectronic device, comprising:  
a microelectronic substrate having a trench formed in a surface thereof;  
a field oxide in the trench, the field oxide extending from the trench, beyond the surface of the substrate;

a gate structure formed on the substrate and having a first polysilicon layer and a second polysilicon layer formed thereon, the gate structure extending from the surface of the substrate by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate; and

a component structure formed on the field oxide and formed from the second polysilicon layer, the component structure having a height relative to the surface of the substrate less than the height of the gate structure.

62. (Previously presented) The microelectronic device of claim 61, further comprising an oxide spacer adjacent the gate structure.

63. (Previously presented) The microelectronic device of claim 61 wherein the component structure is formed on an upper surface of the field oxide.

64. (Previously presented) The microelectronic device of claim 61 wherein the first polysilicon layer has a first layer height relative to the surface of the substrate that is greater than the height that the field oxide extends from the trench beyond the surface of the substrate.

65. (Currently amended) A microelectronic device, comprising:  
a microelectronic substrate having a trench formed in a surface thereof;  
a gate structure formed on the substrate having a first polysilicon layer with a first thickness and a second polysilicon layer formed on the first polysilicon layer and having a second thickness;  
a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than approximately one half of a height of the gate structure formed on the substrate; and  
a component structure formed on the field oxide and formed from the second polysilicon layer having a thickness less than the sum of the first thickness and the second thickness.

66. (Previously presented) The microelectronic device of claim 65, further comprising an oxide spacer adjacent the gate structure.

67. (Previously presented) The microelectronic device of claim 65 wherein the component structure is formed on an upper surface of the field oxide.

68. (Previously presented) The microelectronic device of claim 65 wherein the first polysilicon layer has a first layer height relative to the surface of the substrate that is greater than the height that the field oxide extends from the trench beyond the surface of the substrate.

Amendments to the Drawings:

The attached sheet of drawings includes changes to Figure 2H. Figure 2H has been amended to be consistent with Figures 2F and 2G.

Replacement sheets for Figures 1-3 are also attached.

Attachments: Replacement Sheets  
Annotated Sheet Showing Changes